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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,572	11/12/2003	Kazuaki Sakurada	9319G-000593	8250

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EXAMINER	
TALBOT, BRIAN K	

ART UNIT	PAPER NUMBER
1792	

MAIL DATE	DELIVERY MODE
12/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,572	SAKURADA, KAZUAKI	
	Examiner	Art Unit	
	Brian K. Talbot	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/4/07 has been entered.

2. Claims 2 and 9-12 have been canceled. Claims 1 and 3-8 remain in the application.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

4. Claims 1,2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 08-236,908 in combination with Speakman (6,503,831) (a) alone or (b) further in combination Nagano et al. (5,795,794).

JP 08-236,908 teaches manufacturing of printed circuit boards with uniform thickness in which an insulating layer can be formed between fine pitch conductor patterns. The step of applying the insulating layer can be performed by electrostatic spraying and a contact hole can be formed thereafter by photolithography (abstract).

JP 08-236,908 fails to teach applying the conductor patterns and insulating layer by a droplet jetting method.

Speakman et al. (6,503,831) teaches forming microvias used in printed circuit applications where one requires interconnection between circuits that are laid one on top of the other making use of an interlayer dielectric isolation. Conventional holes are machined in the interlayer to provide access from the top layer circuit to the bottom layer circuit. Ink jet printing provides a means for achieving such microvias by printing discrete areas of material such as an interlayer dielectric on top of the metal contact leaving holes at strategic positions. A second printhead may then be employed to fill the printed holes with an appropriate material. A third head is used to form the top conductor layer (col. 33, lines 5-20). This technique of ink-jetting circuitry is advantageous as it eliminated the need for expensive via forming techniques such as photolithography and etching (col. 16, lines 60-65). The layers are dried and heating to form the patterns. UV radiation is utilized to cure the coated material or to be utilized for other treatments step including surface pre-treatment (col. 38, lines 44-64). A surface wetting layer can be applied to the surface of a substrate to provide wetting and non-wetting areas for subsequent deposition (col. 33, lines 49-60). The conductive material includes particulates as well as colloids including metals such as gold, silver, etc. (col. 4, lines 50-60).

(a) Therefore it would have been obvious for one skilled in the art at the time the invention was made to have modified JP 08-236,908 multilayered printed circuit board process by forming the conductive and/or insulating layers by a ink-jetting process as evidenced by Speakman (6,503,831) with the advantages associated therewith, i.e. avoiding CMP to form a

planar level as well as eliminating the need for via formation as detailed by Speakman (6,503,831) above.

(b) JP 08-236,908 in combination with Speakman (6,503,831) fail to teach specifically "completely filling" the cavity with the second dielectric layer.

Nagano et al. (5,795,794) teaches a process whereby two dielectric layers are applied. The first dielectric layer having an unevenness with valleys and the second subsequent layer filling in those valley to provide a flat even surface (abstract and col. 3, line 60 – col. 4, line 8).

Therefore it would have been obvious for one skilled in the art at the time the invention was made to have modified JP 08-236,908 in combination with Speakman (6,503,831) by forming the dielectric layers to produce a flat even surface as evidenced by Nagano et al. (5,795,794) with the expectation of achieving similar success, i.e. producing a flat even surface.

With respect to claim 6 and the size of the droplets, it is the Examiner's position that this is a "result effective" variable which can be optimized by a practicioner in the art through routine experimentation and therefore does not render as a patentably difference absent a showing of criticality regarding the size of the droplets.

5. Claims 3-5,7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 08-236,908 in combination with Speakman (6,503,831) (a) alone or (b) further in combination Nagano et al. (5,795,794) still further in combination with JP 10-221,698 and JP 11-163,499.

JP 08-236,908 in combination with Speakman (6,503,831) (a) alone or (b) further in combination Nagano et al. (5,795,794) fail to teach measuring and forming data on the circuitry to control the deposition of the insulating layer.

JP 10-221,698 teaches controlling paste quantities upon a substrate by utilizing a computer system to control the distance between the nozzle and the substrate (abstract).

JP 11-163,499 teaches controlling ink-jet deposition by connecting the ink jetting system to a computer and forming graphic information regarding the deposition of the conductive and insulative coating materials.

Therefore it would have been obvious for one skilled in the art at the time the invention was made to have modified JP 08-236,908 in combination with Speakman (6,503,831) (a) alone or (b) further in combination Nagano et al. (5,795,794) multilayer printed circuit board process by utilizing a computer to measure and input data as evidenced by JP 10-221,698 and JP 11-163,499 because of the advantages associated with computer controlled system, i.e. increased precision/accuracy of deposition. Furthermore, it is well settled that it is not invention to broadly provide a mechanical or automatic means to replace a manual activity which has accomplished the same results. *In re Venner and Bowser* 120 USPQ192.

Response to Amendment

6. Applicant's arguments filed 10/4/07 have been fully considered but they are not persuasive.

Applicant argued that the prior art failed to "completely" fill the insulating film to be uniformly even as it has V-shaped gaps.

The Examiner disagrees. JP 08-236,908 depicts the v-grooves formed in Fig. 1b are filled completely in Figs. 1C-1E.

Furthermore, Nagano et al. (5,795,794) teaches this limitation of completely filling the unevenness of a first dielectric layer with a subsequent dielectric layer to produce a flat even surface.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian K. Talbot whose telephone number is (571) 272-1428. The examiner can normally be reached on Monday-Friday 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy H. Meeks can be reached on (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

B K Talbot 12/11/07

Brian K Talbot
Primary Examiner
Art Unit 1762

BKT